

IN THE CLAIMS

Please amend the Claims as follows:

1 (Currently Amended). A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed ~~at the center~~ in a central area thereof;

a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;

a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on ~~the second surface of the resin layer of the substrate~~;

an adhesive attached to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the second semiconductor chip being attached to the adhesive;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on ~~the second surface of~~ the resin layer ~~of the substrate~~;

an encapsulate for encapsulating ~~up~~ the aperture ~~of the~~ substrate, the first and second semiconductor chips, and the first and second conductive wires;~~and~~

~~a plurality of conductive balls coupled to the electrically conductive patterns formed on the second surface of the resin layer of the substrate.~~

2 (Currently Amended). The semiconductor package in accordance with Claim 1 wherein each of first conductive wires ~~for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate~~ are stand off stitch bonded.

3 (Currently Amended). The semiconductor package in accordance with Claim 1 wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip ~~so that the maximum curved portion of the first conductive wire is placed on the electrically conductive pattern.~~

4 (Original). The semiconductor package in accordance with Claim 3 wherein a conductive ball is coupled to the input/output pad of the first semiconductor chip and the first conductive wire is stitch-bonded to the conductive ball.

5 (Currently Amended). The semiconductor package in accordance with Claim 3 wherein each of the plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns ~~formed on the second surface of the~~ resin layer of the substrate are normal wire bonded.

6 (Currently Amended). The semiconductor package in accordance with Claim 3 wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip ~~so that the maximum curved portion of the second conductive wire is placed on the electrically conductive pattern.~~

7 (Original). The semiconductor package in accordance with Claim 6 wherein a conductive ball is fused to the input/output pad of the second semiconductor chip and the second conductive wire is stitch-bonded to the conductive ball.

8 (Currently Amended). The semiconductor package in accordance with Claim 1 further comprising a ~~plate-shaped~~ conductive thin film formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate.

9 (Currently Amended). The semiconductor package in accordance with Claim 8 wherein the electrically conductive patterns are formed on the first and second surfaces of the resin layer and are connected through at least one conductive via.

10 (Original). The semiconductor package in accordance with Claim 9 wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

11 (Currently Amended). The semiconductor package in accordance with Claim 1 wherein the adhesive is silicon having an adhesive layer formed on a top and bottom surface ~~of the~~ thereon.

12 (Original). The semiconductor package in accordance with Claim 1 wherein the second semiconductor chip has an insulating layer formed on the first surface thereof.

13 (Original). The semiconductor package in accordance with Claim 1 wherein the horizontal width of the second semiconductor chip is wider than that of the first semiconductor chip.

14 (Currently Amended). A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at ~~the center~~ a central area thereof;

a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;

a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on ~~the second surface of~~ the resin layer ~~of the substrate~~;

a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon;

means coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the

electrically conductive patterns formed on ~~the second surface of~~
the resin layer ~~of the substrate~~;

means for encapsulating ~~up~~ the aperture of the substrate,
the first and second semiconductor chips, and the first and
second conductive wires; ~~and~~

~~a plurality of conductive balls coupled to the electrically
conductive patterns formed on the second surface of the resin
layer of the substrate.~~

15 (Currently Amended). The semiconductor package in accordance with Claim 14 wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip so that ~~the a~~ a ~~maximum~~ curved portion of the first conductive wire is placed on the electrically conductive pattern.

16 (Currently Amended). The semiconductor package in accordance with Claim 14 wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip so that ~~the a~~ a ~~maximum~~ curved portion of the second conductive wire is placed on the electrically conductive pattern.

17 (Currently Amended). The semiconductor package in accordance with Claim 14 further comprising a ~~plate-shaped~~ conductive thin film formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate.

18 (Original). The semiconductor package in accordance with Claim 17 wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

19 (Original). The semiconductor package in accordance with Claim 14 wherein the second semiconductor chip has an insulating layer formed on the first surface thereof.

20 (Cancelled).

21 (Cancelled).

22 (Cancelled).

23 (Cancelled).

24 (Cancelled).

25 (Cancelled).

26 (Cancelled).

27 (New). A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed in a central area thereof;

a thin conductive film placed over the aperture and coupled to the electrically conductive patterns on the first surface of the resin layer;

a first semiconductor chip having a first surface coupled to the thin conductive film and a second surfaces having a plurality of input/output pads formed thereon;

a second semiconductor chip having a first surface coupled to the first semiconductor chip and a second surface having a plurality of input/output pads formed thereon;

an encapsulate for encapsulating the aperture and the first and second semiconductor chips.

28 (New). A semiconductor package in accordance with Claim 27 further comprising a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer.

29 (New). A semiconductor package in accordance with Claim 27 further comprising a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer.

30 (New). A semiconductor package in accordance with Claim 27 further comprising an adhesive attached to the second surface of the first semiconductor chip.

31 (New). A semiconductor package in accordance with Claim 27 further comprising a plurality of conductive balls coupled to the electrically conductive patterns formed on the second surface of the resin layer.